Remarks

Reconsideration of this Application is respectfully requested.

Claims 15-26 are pending in the application, with claims 15, 20 and 24 being the independent claims.

Attached hereto is a marked-up version of the changes made to the disclosure and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

Based on the above Amendment and the following Remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

1. Objection to the Specification - 35 U.S.C. §132

(a) The Action objects to the amendment filed December 13, 2001 as introducing new matter into the disclosure. According to the Action, the terms "common mask" and "circuit mask", which are not found in the original disclosure, are new matter. This objection is respectfully traversed.

The term "common mask" describes a mask used to form a non-customized layer, and the term "circuit mask" describes a mask used to form a customized layer. **Introduction of the words "common" and "circuit" does not constitute new matter.** The words "common" and "circuit" were added to the application **merely to provide names for the masks that are used to form the non-customized and customized layers respectively**. This was done to clarify the disclosure and claims, thereby better complying with the first and second paragraphs of 35 U.S.C. §112.

The original disclosure at page 1, line 27 to page 2, line 13 (as editorially amended for clarity by the Amendment filed December 8, 2000 and in this amendment) states " In the embedded array system, a layer is provided in which functional elements or devices such as MOS transistors, etc. are formed by using a previously-designed and manufactured mask, and each of the wiring layers for interconnecting the plurality of functional devices with one another is formed over the layer in which the functional elements or devices are formed. Incidentally, each of the wiring layers is normally hereinafter called a "customized layer" because it is designed for each user. On the other hand, the layer in which the functional devices are formed, is hereinafter called a "non-customized layer" because it is used on a general-purpose basis."

Thus, masks used to form non-customized layers have been named "common masks". One or more common masks are used to prepare the non-customized layers forming the CPU block 31, the peripheral blocks 32, the random logic blocks 33, and the gate array block 34. The CPU, peripheral blocks and random logic blocks are dedicated macro cells that are already wired internally. The gate array block initially comprises a plurality of basic gates or cells 41 which are not connected to each other. The interconnections for the gate array block are designed independently from the design and fabrication of the functional blocks and the gate array block. After design of the interconnections has been completed, one or more circuit masks are used to prepare the customized layers forming the interconnections between the basic gates 41 comprising the gate array block 34. This results in a substantial reduction in the time required to design and fabricate the integrated circuit.

Both types of masks are discussed in the disclosure, as filed, but were not separately identified. The added words "common" and "circuit" identify which masks are used to prepare

the "non-customized" and "customized" layers. No new elements or components have been added to the disclosure or drawings, and therefore the prohibition in 35 USC 132 against the addition to an application of new matter has not been violated.

(b) The action states in the second paragraph on page 2 "The specification as originally filed does not appear to teach a "common" mask of any type, and in particular the specification does not teach a "common" mask for forming the gate array block and the plurality of functional blocks, as now recited in the claims." However, the word "common" should not be construed as meaning that a single mask must be used to form the functional elements and the gate array block; rather this word refers to the mask or masks used to form layers which are not customized as opposed to circuit masks which form only customized layers. Thus, claim 15 recites "employing at least one common mask to form a plurality of functional blocks and a gate array block".

Referring to the Summary of the Invention, page 4, lines 8-15, the first step in Applicants' novel method of manufacturing a semiconductor integrated circuit is placing a basic cell block (or gate array block, see page 8, line 10) and a plurality of functional blocks within a predetermined area of a semiconductor chip. The second step is to independently design the circuits for the gate array block. The third step is to electrically connect the basic cells located within the gate array block.

More specifically, the IC chip is divided into a function cell block layout area (CPU block 31, peripheral blocks 32 and random logic blocks 33) in which the circuit is already determined and no change is to be made in the circuit, and another area in which a plurality of unconnected basic cells 41 are arranged in line to form the gate array block 34. (Page 7, lines 21-

27). Upon completion of this IC design, design and fabrication of a common mask (or masks) for fabrication of the non-customized layer (or layers) is begun. (Page 8, lines 4-7). **Thus, at least one mask is used to form the complete CPU block 31, peripheral blocks 32, random logic blocks 33 and the gate array block 34 , the gate array block at this stage consisting of unconnected basic cells.** Thereafter, the basic cells 41 of the gate array block 34 are interconnected and connections are made to and between the functional elements by use of a circuit mask (or masks) which forms the customized layer (or layers). (page 8, lines 8-13) Summarizing, the gate array block 34, which has unconnected basic cells 41, is formed in the non-customized layer in a first step by the common mask (or masks), whereas the connections of the gate array block 34 are made in a second step using a circuit mask (or masks) subsequent to the first step.

2. Claim Rejections - 35 U.S.C. §112, first paragraph

(a) Claims 1-6 and 9-14 stand rejected under 35 U.S.C. §112, first paragraph. As discussed above regarding the objection to the specification, the claims now recite that "at least one common mask" forms the functional blocks and the gate array ~~block~~. This recitation is supported by the disclosure of a single mask forming a single layer, the chip comprising a plurality of such layers. As also discussed above, the recitation of "common" and "circuit" mask are merely labels used for identifying the masks associated with the "non-customized" and "customized" layers discussed in the disclosure. Accordingly, it is respectfully submitted that the claims comply with the first paragraph of section 112.

(b) Claims 1-6 and 9-12 have been rejected under 35 U.S.C. §112, first paragraph on the ground that no teaching is provided to explain to one of ordinary skill how to form a gate array

block and a plurality of functional blocks with "a" common mask. However, as discussed above, the disclosure is not limited to the use of a single mask for forming either the non-customized or customized layer or layers. Referring to page 4, lines 17-27 and page 5, lines 6-23, it is clear that Applicants contemplated the use of a plurality of masks in the manufacture of the functional blocks and the metal wiring layers. Nevertheless, a single mask may be appropriate for the fabrication of certain IC's, and the claims have been properly drafted to include this possibility.

3. Claim Rejections - 35 U.S.C. §103

Claims 1, 5-6 and 12 are rejected under 25 U.S.C. §103(a) as being unpatentable over Andrews et al. (hereinafter "Andrews") and Tavana et al. (hereinafter "Tavana") in view of Kean and Kawashima. These claims have been cancelled in favor of new claims 15-26.

Andrews teaches a hybrid integrated circuit 400 with an array 402 of programmable logic cells (PLC) surrounded on three sides by programmable I/O cells 404 and an outermost ring of pads 406. One side of the PLC array 402 is bounded by field programmable gate array (FPGA) application specific block (ASB) interface hardware 412 that allows the PLC array 402 to interface with an application specific block 408 which can be implemented with mask-programmed devices (MPD)-type logic. (Fig. 4, col. 3, lines 38-48). Thus, Andrews discloses that regions of FPGA-type logic (for example, 402) can be combined with regions of MPD-type logic (for example, 408) on a single chip. (col. 3, lines 7-19). Andrews discloses that the FPGA-type logic can be implemented with "any suitable type of field programmable logic" and that the MPD-type logic an be implemented with "any suitable type of mask-programmable logic." (col. 5, lines 16-23).

Tavana teaches a monolithic circuit device 10 with a field programmable gate array portion 12 and a mask-defined application specific logic area 14. (page 8, lines 17-21 and Fig. 2) Programmable 28 and mask-defined 30 interconnections are used as routing to interconnect the FPGA 12. (page 10, line 12 - page 11, line 2)

Kean teaches a field programmable gate array 10 with a plurality of cells 12 arranged in rows and columns. (see, for example, col. 12, lines 11-26 and Fig 1)

Kawashima teaches a semiconductor integrated circuit, including a technique for increasing the density of integration of input and output buffers in the semiconductor integrated circuit (col. 1, lines 10-17).

As recited in claim 15 and described in the disclosure, at least one common mask is used to form the non-customized layer of an integrated circuit, which can include, for example, the CPU core block 31, the peripheral block 32, the random logic blocks 33, and the gate array block 34. The gate array block 34, as prepared by the common masks, is made up entirely of basic cells 41 with no interconnections. Circuits corresponding to the desired function of the gate array block are designed and the interconnections forming the circuitry are established by a circuit mask.

This method of manufacturing a semiconductor integrated circuit permits the engineer to first design and prepare common masks for fabricating the non-customized portions of an IC (functional elements 31-33) and a gate array block 34 (consisting only of unconnected basic cells 41). The second step of designing the customized circuits for the gate array block is carried out at any time, independently of the first step. Thereafter, the IC is completed by adding the circuit

connections to the gate array block using circuit masks. It is understood that this method results in a considerable saving of time over conventional methods of manufacturing integrated circuits.

Claim 15 recites "employing at least one circuit mask to establish electrical connections between the basic cells."

In the Action dated September 13, 2001, the Examiner cites Andrews as teaching a field programmable gate array and cites Kean as teaching that field programmable gate arrays are programmed by establishing electrical connections between the cells. Although the Action is correct in stating that the field programmable gate arrays are programmed by the user designing and establishing electrical connections, it is respectfully submitted that the field programmable gate arrays, such as those taught in Andrews, Kean and Tavana, are not programmed using a circuit mask. As discussed in Tavana, mask programmed gate arrays are programmed with a mask which establishes custom metallization layers in order to connect transistors located within a semiconductor substance to perform a particular logic function. (page 1, lines 31-36). This is in contrast to a field programmable gate array which has, in one embodiment, many pass transistors which can be turned on or off to connect or not connect corresponding lines to logic circuits, to other lines, or to input/output pads. (page 2, lines 15-17). Andrews also discusses the differences between a mask programmed gate array and a field programmable gate array (col. 1, line 9 to col. 2, line 15).

Andrews fails to teach the use of functional blocks with gate array blocks. Andrews teaches a hybrid IC 400 having a field programmable array 402 surrounded by sets of FPGA-ASB interface hardware 412 that allows the field programmable array 402 to interface with an application specific block 408, which is implemented using mask programmed device logic. (col.

3, lines 38-50 and Fig. 4). In effect, Andrews uses a combination of mask programmable and field programmable devices.

Accordingly, claim 15 distinguishes over and is allowable over the cited prior art. Claims 16-19 depend from claim 15 and are allowable as depending from an allowable claim. New claim 20 is an apparatus claim with features corresponding to claim 15. Thus, claim 20 is allowable for the reasons discussed above in regard to claim 15.

New independent claim 24, similar to claim 15, recites that at least one common mask establishes the functional blocks and the gate array block and at least one circuit mask establishes the interconnections of the basic cells in the gate array block. Claim 27 depends from claim 26 and specifies that the circuits are designed while the "non-customized" layer is being formed. Claim 28 also depends from claim 26 and specifies that the circuit are not designed until the "non-customized" layer is complete. The prior art does not teach such a manufacturing method.

4. Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance with claims 15-26.

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is hereby invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment is respectfully requested.

Respectfully submitted,

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Version With Markings To Show Changes Made

In The Disclosure:

Please amend the disclosure as follows:

Page 1, replace the paragraph beginning on line 27 with the following rewritten paragraph:

The embedded array system in contrast to the above-described gate array system, standard cell system and full custom system has the following characteristics. Namely, according to the embedded array system, dedicated macro cells such as a CPU, a RAM, etc. are embedded in a base array at a design state of an IC layout. [A] In the embedded array system, a layer is provided in which functional elements or devices such as MOS transistors, etc. are formed [,is formed] by using a previously-designed and manufactured mask, and each of the wiring layers for interconnecting the plurality of functional devices with one another is formed over the layer in which the functional elements or devices are formed. Incidentally, each of the wiring [layer] layers normally hereinafter call a "customized layer" because it is designed for each user. On the other hand, the layer in which the functional devices are formed, is hereinafter called a "non-customized layer" because it is used on a general-purpose basis.

Page 6, replace the paragraph beginning on line 26 with the following rewritten paragraph:

In order to previously design and manufacture the common [mask] masks for the non-customized [layer] layers, the following two conditions must be met. The first condition is as follows: It is necessary to fix patterns for functional elements or devices such as transistors for constituting each non-customized layer and avoid changes in patterns after the design and fabrication of the mask are started. Further, the second condition is as follows: Interconnections in each wiring layer used as a customized layer are suitably formed in association with the non-

customized layer so that desired functions are obtained. Namely, if basic gates (also called "basic cells") based on the gate array system are partially embedded in the IC designed by the standard cell system or full custom system, and the plurality of embedded basic gates are electrically connected to one another and utilized in combination so as to implement the desired functions, then the common masks [mask] used for the non-customized layers [layer] can be designed and fabricated prior to the formation of the customized layer even in the case of the IC designed by the standard cell system or full custom system.

Page 7, replace the paragraph beginning on line 17 with the following rewritten paragraph:

A process for designing such an IC as to allow the common masks [mask] for the non-customized layers [layer] to be designed and fabricated prior to the formation of the customized layer, using the standard cell system or full custom system will next be explained.

Page 7, replace the paragraph beginning on line 28 with the following rewritten paragraph:

Next, design resources based on the gate array system are blocked to effect layout design on the area having the potential of change in circuit. The layout of the entire IC is designed while the blocked design resources based on the gate array system are being captured by a CAD (Computer Aided Design) of the standard cell system or full custom system. Upon completion of the layout design of the entire IC, the design and fabrication of the common masks [mask] related to the non-customized layers [layer] is started.

Page 8, replace the paragraph beginning on line 8 with the following rewritten paragraph:

Thereafter, when the contents of the circuit is determined in the area having the potential of the change in circuit, each gate array block corresponding to a basic cell block is again laid out using the CAD of the gate array system. The design and fabrication of a circuit mask corresponding to each customized layer are started based on the re-laid out gate array block. Incidentally, the gate array block whose circuit has been determined, is laid-out in a design based on the non-customized [layer] layers formed by the previously-designed and fabricated common masks [mask]. Namely, the gate array block preceding the determination of the circuit and the gate array block subsequent to the determination of the circuit are respectively made up of the same basic gate comprised of basic gates identical in number in both the vertical and horizontal directions.

Page 10, replace the paragraph beginning on line 4 with the following rewritten paragraph:

Since diffused layers, polysilicon layers, metal wiring layers, etc. are conventionally formed after the design and fabrication of the masks when the IC is designed by the standard cell system or full custom system, it normally took several months to complete the IC. On the other hand, according to the IC chip 1 in an embodiment of the present invention, it is possible to previously design and manufacture the common masks [mask] corresponding to the non-customized layers [layer] during a logic-simulation stage, for example. Further, the design work such as the logic simulation or the like is continuously performed in parallel with the design and fabrication of the common masks [mask]. Thereafter, when the corresponding circuit for the gate array block 34 has been determined, the layout of the gate array block 34 is designed again, and the circuit mask corresponding to a customized layer is designed fabricated.

Page 10, replace the paragraph beginning on line 20 with the following rewritten paragraph:

When the fabrication of the non-customized layers [layer] is completed before the start of the fabrication of the customized layer, for example, a TAT required from the start of the fabrication of the customized layer to the completion of formation of all the layers of the IC chip 1 takes the same several weeks as the manufacturing period of the customized layer. Namely, the period from the completion of the design of the IC to the completion of the fabrication of the IC chip can be greatly reduced by several months to several weeks as compared with the prior art in which the IC has been designed using the standard cell system or full custom system.

Page 11, replace the paragraph beginning on line 1 with the following rewritten paragraph:

According to the IC chip 1 related to the embodiment of the present invention, when a circuit change occurs in the gate array block 34, the designer of the IC chip can cope with such a circuit change by redesigning only the gate array block 34 while the contents of the circuit of the non-customized layers [layer] is maintained. That is, only the circuit mask related to the gate array block 34 is changed in design. Thus, the circuit change of the gate array block 34 can be completed in a short period of time.

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